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DESIGN OF LOW DELAY 4:2 COMPRESSOR FOR MULTIPLIERS

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Abstract—In this paper, energy-efficient design for a 4:2 compressor is proposed which utilizes 28 transistors. This design makes use of 4 transistor XOR module and a 2x1 mux module using transmission gates. The XOR- MUX architecture for the 4:2 compressor lowers the already low power consumption of the compressor. The methodology used for designing this architecture is CMOS modeling, in which each module of the architecture is designed using the least number of CMOS transistors.. The proposed design of the compressor, when implemented on 45nm technology using the Microwind tool, provided a maximum output delay of 650ps which is quite less than its predecessor designs which showed a delay of 920.1ps. This low power design will help the design of low energy and fast multipliers.

Keywords: Multiplier, compressor, high speed, low power, XOR-MUX module

I. INTRODUCTION

In digital devices, the role of a multiplier is to multiply two n-bit numbers. It is an operation that is widely used in electronic devices such as digital measuring instruments, microprocessors, microcontrollers, etc. The current multipliers are of two types, serial multipliers which are small in size but are quite slow. On the other hand, we have parallel multipliers that take up a large area but provide high speed. Designing a multiplier that is of high speed and covers up less area is the requirement so that modern-day devices can be both fast and small.

When it comes to designing small multipliers the difference between the parameters of various designs is not much. The difference comes to light when we start moving towards high bit multipliers like 8 bit and more and designing new circuits for these multipliers will be a highly lengthy and complicated process and will lead to large Boolean equations. Thus the key to designing these multipliers is following the basic principles of VLSI i.e. regularity, modularity, and locality.

In parallel multipliers, there are various multipliers like Wallace tree multipliers which are very fast but take up a large area and are high in complexity. Then there are other designs such as array multipliers which consume less area but have propagation delay more than Wallace tree multiplier.

To achieve the point where we have less output delay and the area covered by the module is also less the design of compressors comes up. Compressors are high-speed processing devices that are used in multipliers to reduce the number and size of modules used. The compressors used in multipliers are made by integrating two successive Full adders and minimizing their logic.

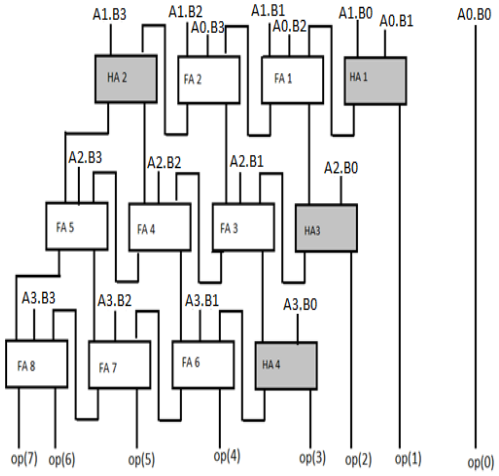

Fig 1: Design of an Array Multiplier

II. COMPRESSOR

A compressor is a combinational circuit that compresses the number of partial products to a lower number of partial products. For example, a 4:2 Compressor compresses 4 partial products into 2 partial products[2]. A 4:2 Compressor

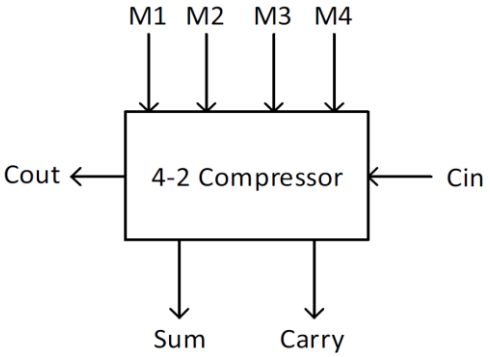

Fig 2: Block Diagram of Compressor

is depicted by the block diagram shown in Fig 2.

The role of a compressor in a multiplier is to decrease the amount of circuitry in the module which leads to lowering of the maximum output delay of the circuit. The compressor also leads to a decrease in power consumption as the components used in the module is low. This compressor when replaces multiple modules of the multiplier leads to a

cascading effect in the decrease of the parameter values of the multipliers.

This Compressor has 5 inputs M1, M2, M3, M4, and Cin where M1 to M4 are partial products and Cin is the carry obtained from a previous module. This compressor consists of 3 outputs Cout, Carry, and Sum. Where Cout acts as carry for the upcoming module[3]. Fig 3 shows the architecture of

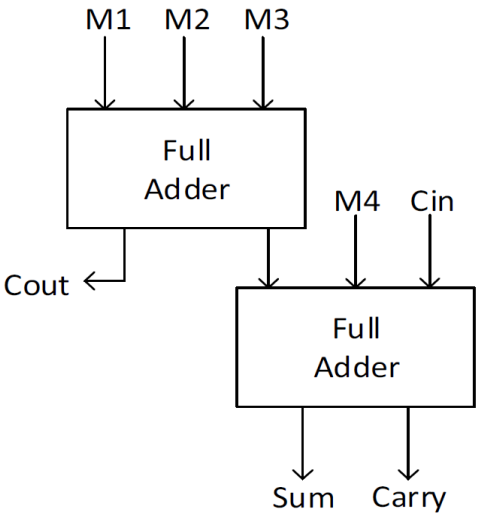

Fig3: Basic Module of a 4:2 Compressor

the basic module of a compressor.

In literature, various architectures have been referred to for implementation of a 4:2 compressor but the two that have been commonly used. The first one involves the use of XOR modules and a 2x1 MUX where there are three XOR modules and two 2x1 Multiplexer modules[4]-[7]. This architecture is denoted in Fig 4.

The other architecture of the 4:2 compressor involves the use

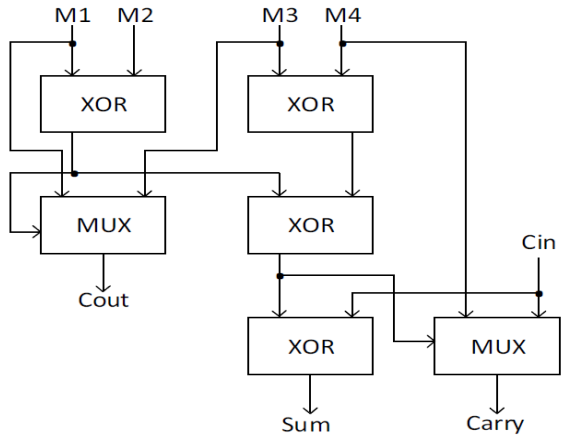

Fig 4: Architecture using XOR module

of an XOR-XNOR module and 2x1 MUX where there are two XOR-XNOR modules and four 2x1 MUX. In this architecture, there is the use of an additional inverter in the XOR module to convert the XOR output to XNOR [8]-[11]. This architecture is denoted in Fig 5.

In the XOR module architecture which is used in this paper, the logic simplification can be seen when we count the

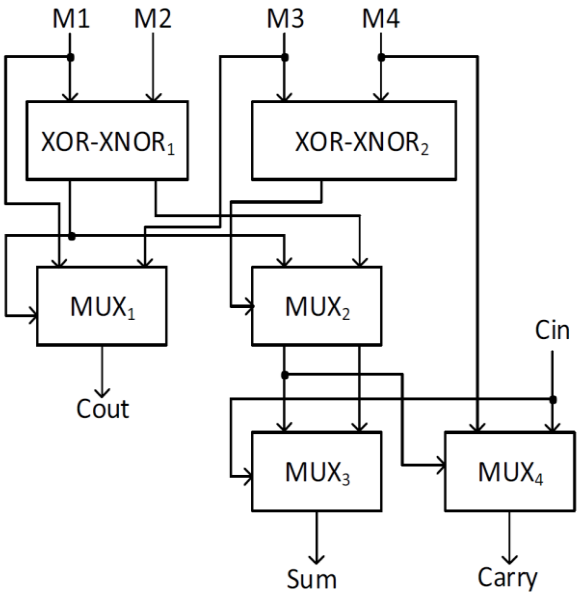

Fig 5: Compressor architecture using XOR - XNOR module

number of stages the output takes to be propagated. The basic design which when used took 3 stages to generate Cout, 4 stages to generate sum, and 5 stages to generate Carry. When this architecture is used then the number of stages of Cout was reduced from 3 to 2 for Sum from 4 to 3 and for Carry from 5 to 3. This shows that the reduced logical design for the compressor is effective in reducing the delay of the module.

III. Design

The architecture used for the design is the XOR-MUX architecture where there are three 2-input XOR modules and two 2x1 multiplexers [11]. The 2x1 multiplexer is designed

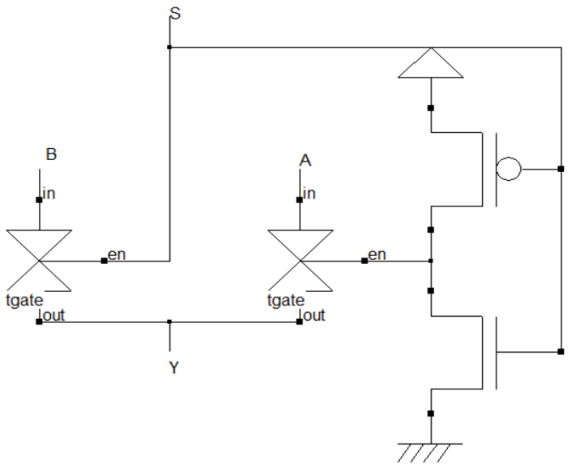

Fig 6: 2x1 MUX using Transmission Gates

using transmission gates as shown in Figure 6.

The XOR module is designed using 4 transistors. This module is then used along with the multiplexer module to

implement a 4:2 compressor. The whole circuit uses a total

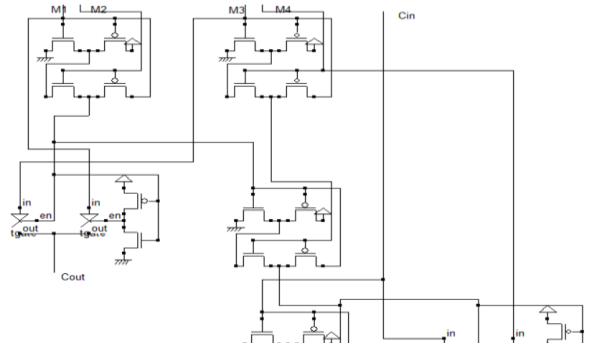

Fig 8: Design of a 4-bit array multiplier

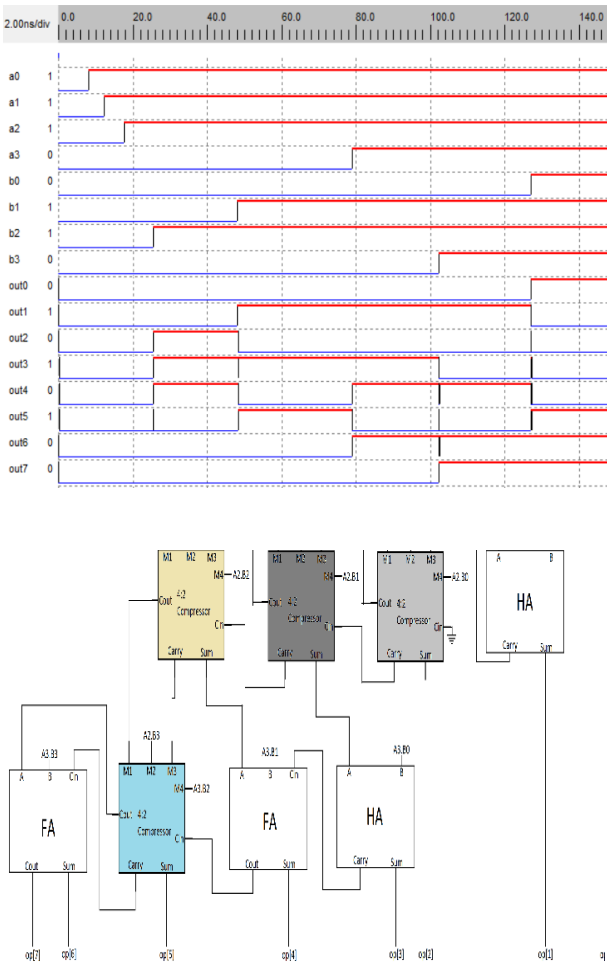

Fig 9: Design of 4 bit multiplier using 4:2 compressors

of 28 transistors and is shown in Figure 7.

IMPLEMENTATION IN 4-BIT MULTIPLIER

The Proposed design was then implemented on a 4-bit multiplier (shown in Fig 9). In this design, the partial products were obtained from passing the input through the array of AND gates then in the next stage [7], the partial products are provided as an input to the adder array which now has been replaced by a faster and low power compressor. Thus, initially the design which used 12 adder circuits has been reduced to a design that uses 4 adder circuits and 4 compressor circuits.

The proposed design, when implemented on a 4-bit multiplier reduces the design of multiplier as shown in figure 9 to the multiplier as shown in figure 10.

RESULT

The proposed compressor design was then verified using the Microwind tool where inputs were applied to M1, M2, M3, M4 & Cin and the corresponding outputs at Cout, Sum, and Carry were obtained. The Input-output waveforms for the proposed design are in Figure 8.

The design showed a delay of 650psfor 45nm design rules.The other designs for similar architecture showed a delay of at least 920.1ps [2]-[7]. The delay for the base design used in Figure 3 was 1310ps [1].

This design when implemented on a 4-bit multiplier was tested for maximum output delay it showed that the delay was 0.187ns whereas the design using adder circuits as

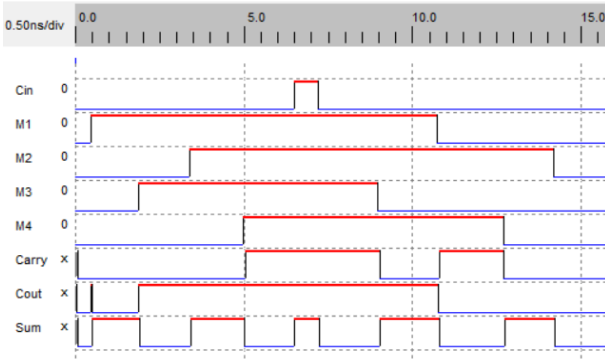

Fig 10: Input-Output waveforms obtained in proposed design

shown in Figure 3 had a delay of 0.271ns the input-output waveforms for the 4-bit multiplier are shown in Figure 11. This shows that the design which used the proposed design of compressor used 0.084ns less i.e., 31% less than the basic design of array multiplier.

CONCLUSION

In this paper, a new design for the 4:2 compressor is presented which uses fewer transistors than its predecessors. With the reduction in transistors, the maximum output delay of the design has also reduced to 650ps for 45nm CMOS design. With these results, we can say that this compressor when implemented on a multiplier will help in the reduction of the propagation delay of the device.

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